REMARKS

Applicant has carefully reviewed and considered the Office Action mailed on May 29, 2002, and the references cited therewith.

Claims1, 7, and 14 are amended, claims1-23 are now pending in this application. Amendment to claims 1, 7, and 14 are made for purposes of clarification based on the Examiner's Rejection and are not believed to introduce any new matter.

§103 Rejection of the Claims

Claims 1-11, 13-17, and 19-23 were rejected under 35 USC § 103(a) as being unpatentable over Horiguchi ("Direct Tunneling Memory..."). It is fundamental that to sustain a § 103(a) rejection, each and every element in the rejected claims must be taught or suggested in the references cited. Applicant's amended claims 1, 7, and 14 recite floating gates having much smaller capacitances than control gates. In contrast, this reduction in capacitance between floating gates and control gates is not taught or suggested in Horiguchi.

The Examiner has asserted that product by process limitations do not structurally distinguish over the references cited, since it is the final product that which is deemed more significant. Applicant's amended claims 1, 7, and 14 produce final products that are distinguishable over Horiguchi, since in Horiguchi produced memory is one in which gate leakage is reduced. Conversely, Applicant's invention produces memory cells and transistors that include floating gates with much smaller capacitances than the control gates.

As stated in the original filed application, much smaller capacitances between the floating gates and the control gates permit a majority of any voltage applied to a control gate to appear across a floating gate thin tunnel oxide. Thus, the devices of the Applicant's present invention can be programmed by tunneling of electrons to and from the silicon substrate at lower control gate voltages than is possible in Horiguchi.

Accordingly, Horiguchi appears to teach and suggest memory where gate leakage is suppressed or reduced. However, Horiguchi does not teach or suggest memory wherein floating gate capacitances are smaller than control gate capacitances. Therefore, the Examiner's rejection with respect to Horiguchi should be withdrawn.

Claims 1-23 were rejected under 35 USC § 103(a) as being unpatentable over Horiguchi in view of Watanabe (U.S. Patent No. 6,133,601) or Hong et al. (U.S. Patent No. 5,625,213). As stated above with respect to Horiguchi, in order to sustain a § 103(a) rejection, each and every element in the rejected claims must be taught or suggested in the references cited. Neither Horiguchi, Watanabe, nor Hong, standing alone or in combination, teach or suggest floating gates having smaller capacitances than control gates, as recited in Applicant's amended claims 1, 7, and 14.

Horiguchi teaches and suggests suppressing gate leakage. Watanabe teaches and suggests preventing variations in capacitance between floating gates and control gates. (Watanabe, col. 8, lines 37-39). Watanabe actually teaches away from Applicant's invention since the teachings of Watanabe produce devices where variations in capacitance between floating gates and control gates are prevented. Whereas, Applicant's invention produces devices wherein floating gates have much smaller capacitances than control gates. Accordingly, Watanabe suggests that variations in capacitance are to be avoided, and therefore, Watanabe cannot be said to teach or suggest floating gates with much smaller capacitances than control gates.

Finally, Hong is directed to a top floating-gate flash EEPROM structure. Hong teaches improving reliability of flash EEPROM during program and erase operations by leaving the source and the drain floating during these operations. (Hong, col. 5, lines 9-14). Hong, does not teach or suggest devices wherein capacitances of floating gates are much smaller than capacitances of control gates.

Thus, the rejections with respect to Horiguchi, Watanabe, and Hong are no longer sustainable and should be withdrawn.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney, Joe Mehrle, at (513) 942-0224 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account

No. 19-0743.

Respectfully submitted,

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Date 8/29/2002 By _____
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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 29 day of August, 2002.

Jane E. Brockschink
Name

_____
Signature